

**Phase Shifter, S-Band, 6 Bit**  
**2.3-4.1 GHz**

**MAPCGM0003**  
Rev C

**Features**

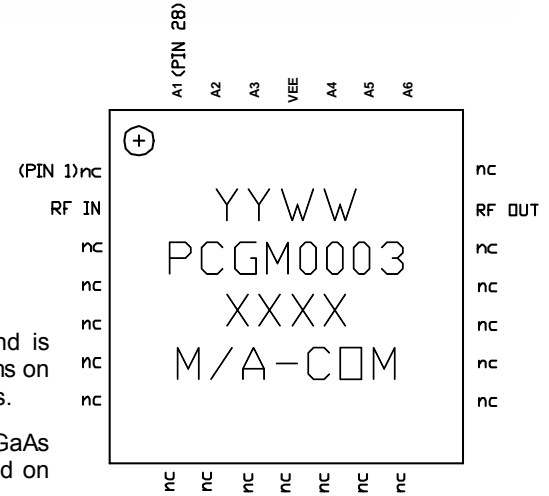
- ◆ 2.3 to 4.1 GHz Operation
- ◆ 6 Bit Phase Shifter
- ◆ 360° Coverage, LSB = 5.6°
- ◆ TTL Control Inputs
- ◆ MSAG™ Process
- ◆ 6mm, 28 Lead, PQFN Package

**Description**

The MAPCGM0003 is a 6-bit Phase Shifter with Parallel TTL Input Control and is packaged in a micro lead package (MLP). This product is fully matched to 50 ohms on both the input and output. This part has 360° of phase coverage in 5.6° increments.

Fabricated using M/A-COM's repeatable, high performance and highly reliable GaAs Multifunction Self-Aligned Gate MSAG™ Process, each device is 100% RF tested on wafer to ensure performance compliance.

M/A-COM's MSAG™ process features robust silicon-like manufacturing processes, planar processing of ion implanted transistors, multiple implant capability enabling power, low-noise, switch and digital FETs on a single chip, and polyimide scratch protection for ease of use with automated manufacturing processes. The use of refractory metals and the absence of platinum in the gate metal formulation prevents hydrogen poisoning when employed in hermetic packaging.



**Primary Applications**

- ◆ Communications
- ◆ Phased Array Radar

**Also Available in:**

Description	DIE	Sample Board (Plastic)
Part Number	MAPCGM0003-DIE	MAPCGM0003-SMB

**Electrical Characteristics  $T_B = 25^\circ\text{C}^1$ ,  $Z_0 = 50\Omega$ ,  $V_{EE} = -5\text{V}$**

Parameter	Symbol	Minimum	Typical	Maximum	Units
Bandwidth	f	—	2.3-4.1	—	GHz
Insertion Loss	IL	4	6	10	dB
Input VSWR (At Reference)	VSWR	—	1.5:1	4.4:1	
Output VSWR (At Reference)	VSWR	—	1.2:1	2.3:1	
RMS Phase Error	RMS	—	6	—	°
RMS Phase Error — Calibrated	RMS	—	3	—	°
Phase Range	$\Delta\Phi$	—	360	—	°
Phase Accuracy — 5.6° Bit	$\Delta\Phi_{REF}^2$	-7.2	-5.6	-4.2	°
Phase Accuracy — 11.2° Bit	$\Delta\Phi_{REF}$	-11.8	-11.2	-8.4	°
Phase Accuracy — 22.5° Bit	$\Delta\Phi_{REF}$	-34	-22.5	-16	°
Phase Accuracy — 45° Bit	$\Delta\Phi_{REF}$	-59	-45	-35	°
Phase Accuracy — 90° Bit	$\Delta\Phi_{REF}$	-98	-90	-84	°
Phase Accuracy — 180° Bit	$\Delta\Phi_{REF}$	-200	-180	-170	°
Phase Accuracy — All Bits	$\Delta\Phi_{REF}$	-390	-360	-340	°
Gain Variation over all Phase Shifter settings	$\Delta G$	—	< 3	—	dB
Digital Supply Current	$I_{EE}$	—	< 10	—	mA
Input Third Order Intercept	ITOI	—	36	—	dBm
Input 1-dB Compression Point	$P_{1dB}$	—	23	—	dBm

1.  $T_B$  = Package Base Temperature
2. All  $\Delta\Phi_{REF}$  values are relative to the Reference State (i.e. All phase bits set to 0V).

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Visit [www.macom.com](http://www.macom.com) for additional data sheets and product information.

### Maximum Ratings<sup>3</sup>

Parameter	Symbol	Absolute Maximum	Units
Input Power	P <sub>IN</sub>	30	dBm
Supply Voltage	V <sub>EE</sub>	-6	V
Junction Temperature	T <sub>J</sub>	170	°C
Storage Temperature	T <sub>STG</sub>	-55 to +150	°C

3. Operation beyond these limits may result in permanent damage to the part.

### Recommended Operating Conditions<sup>4</sup>

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>EE</sub>	-5.2	-5.0	-4.8	V
Control Voltage	A1 thru A6				
Logic High		3	5	5	V
Logic Low		0	0	0.4	V

4. Operation outside of these ranges may reduce product reliability.

### Truth Table<sup>5</sup>

Pin	Designation	Description	Level	State
22	A6	180° Phase Bit : MSB	Logic High	Phase Shift ≈ -180°
23	A5	90° Phase Bit	Logic High	Phase Shift ≈ -90°
24	A4	45° Phase Bit	Logic High	Phase Shift ≈ -45°
25	V <sub>EE</sub>	DC Supply Voltage	-5V	ON
26	A3	22.5° Phase Bit	Logic High	Phase Shift ≈ -22.5°
27	A2	11.2° Phase Bit	Logic High	Phase Shift ≈ -11.2°
28	A1	5.6° Phase Bit : LSB	Logic High	Phase Shift ≈ -5.6°

5. All Phase Bits at Logic Low = Reference State.

### Operating Instructions

This device is static and light sensitive. Operation of the digital circuitry can be impaired under high intensity light, e.g., microscope light.

No voltage sequencing is required to operate this part.



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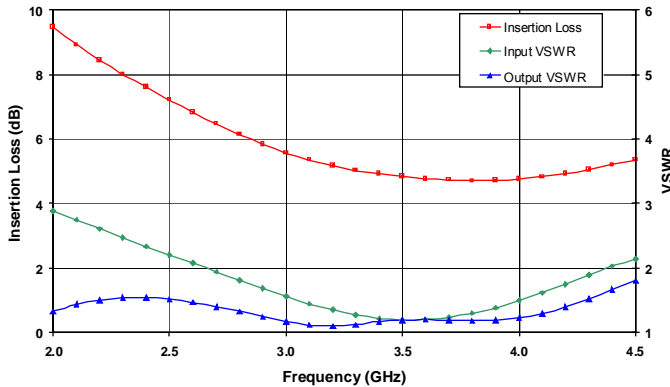


Figure 1. Reference State Insertion Loss, Input and Output VSWR vs. Frequency

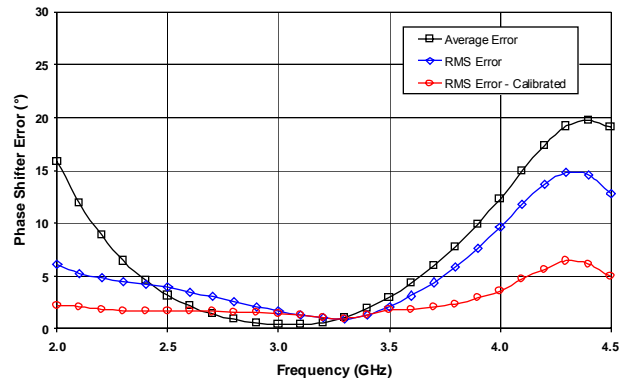


Figure 2. Phase Shifter Figures of Merit: Average Error vs. Reference State, RMS Error and Calibrated RMS Error Over All States

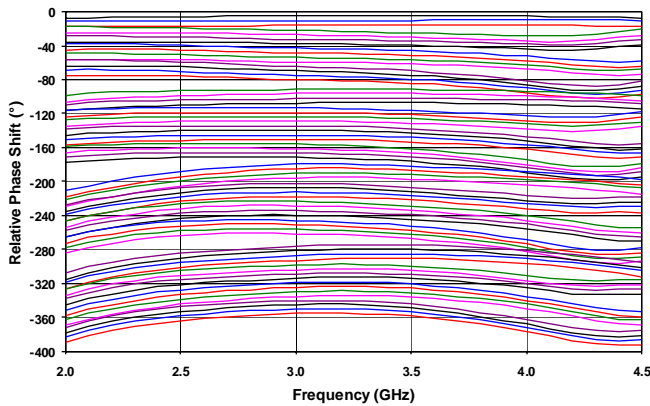


Figure 3. Relative Phase Shift vs. Phase Shifter State

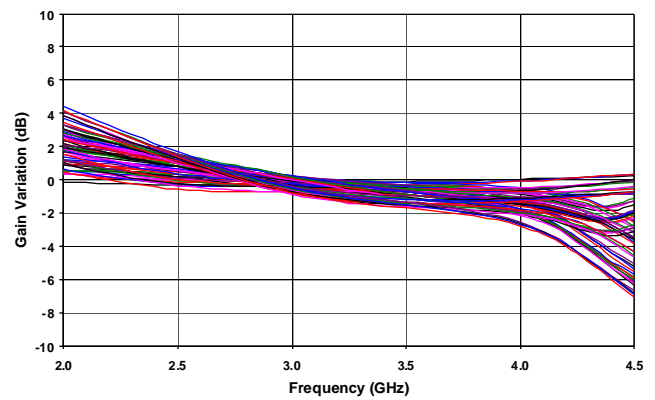


Figure 4. Relative Gain Change vs. Phase Shifter State

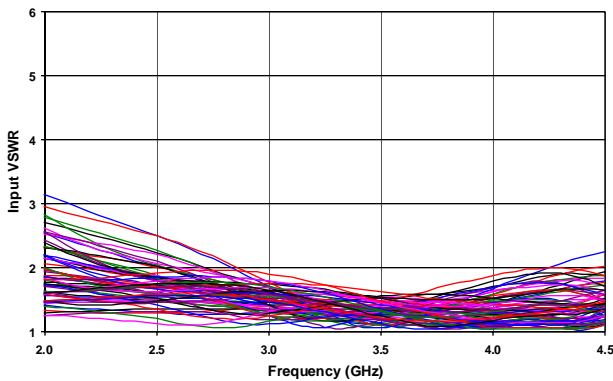


Figure 5. Input VSWR vs. Phase Shifter State

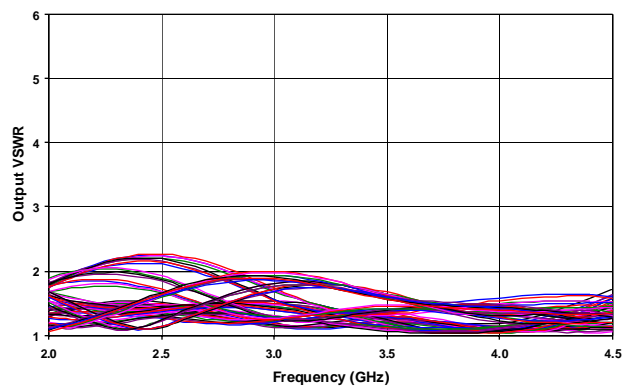
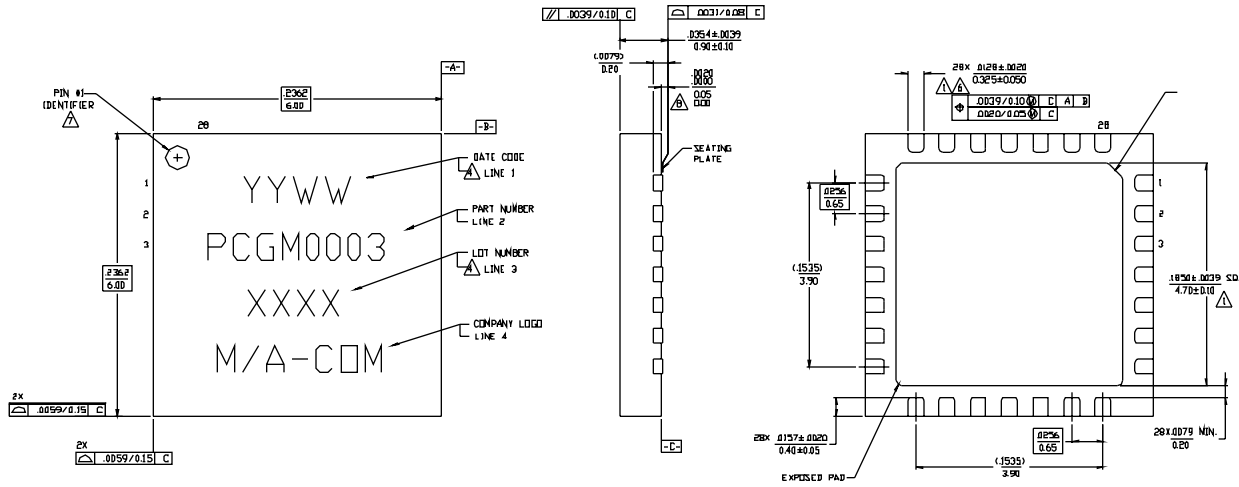


Figure 6. Output VSWR vs. Phase Shifter State

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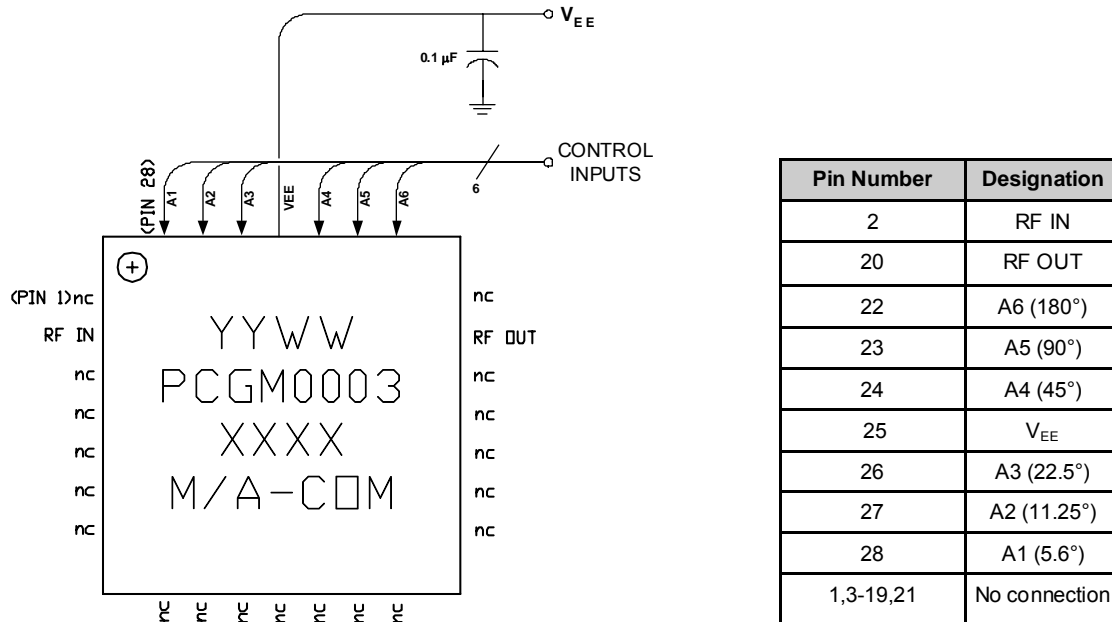
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**Figure 7. PQFN, 6mm, 28 Lead Package Drawing**

Reference JEDEC M0-220 (see <http://www.jedec.org>), VAR. VJJC-3 (Issue E) for additional dimensional and tolerance information.



**Figure 8. Recommended Bias Configuration**

Refer to M/A-COM Application Note **Surface Mounting Instructions for PQFN Packages #S2083\*** for assembly guidelines.

Application Notes can be found by going to M/A-COM's web page (<http://www.macom.com/Application%20Notes/index.htm>) and searching for the required Application Note.

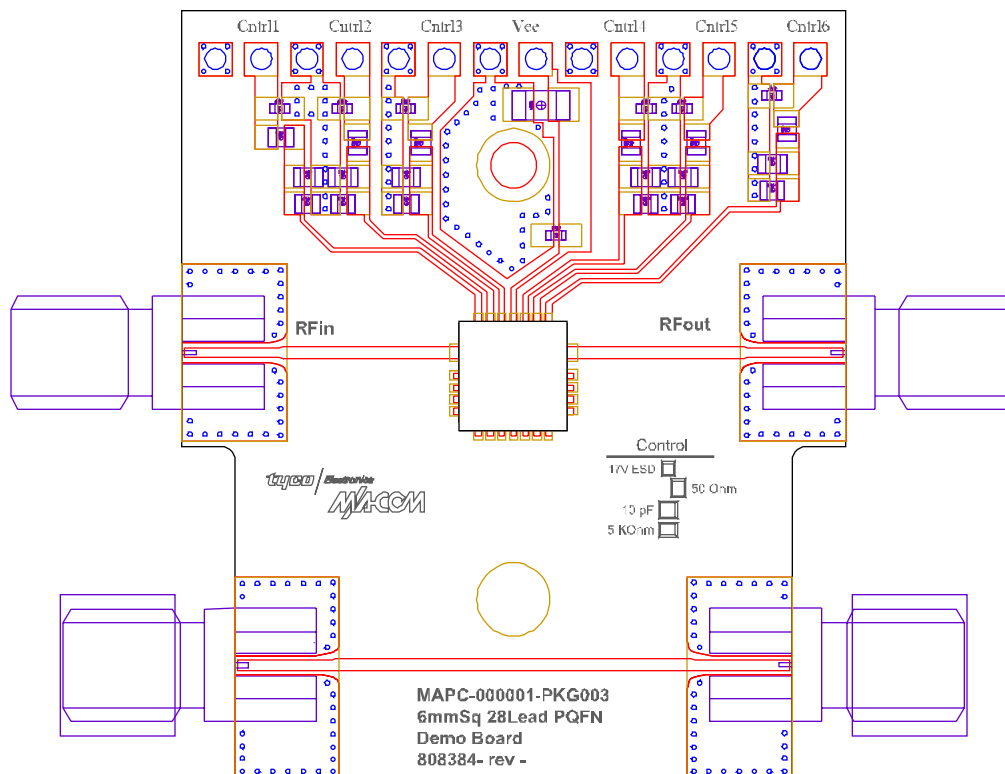


Figure 9. Demonstration Board (available upon request).